

HA-EDA01 FPGA Module

Hardware User's Guide

Rev 1.2

华清科仪（北京）科技有限公司

 **Huatsing Instruments**

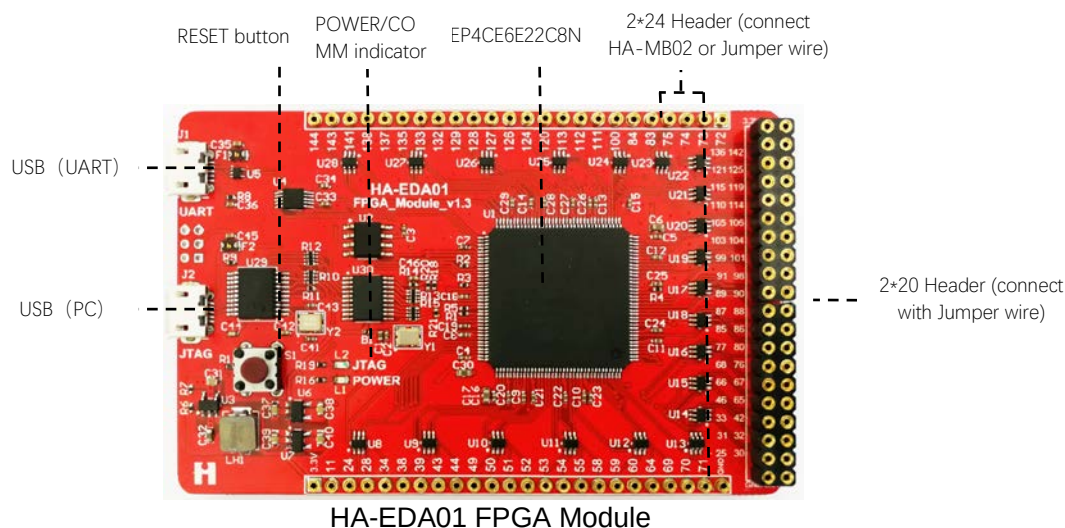
1. Introduction

Thank you for choosing the HA-EDA01 FPGA Module of Huatsing Instruments(HI)!

HA-EDA01 FPGA Module is a compact FPGA board which is designed based on EP4CE6 device. It's a low-cost and easy-to-use platform for learning Altera's Cyclone IV FPGA. This board includes integrated USB-Blaster circuitry for FPGA programming. Abundant I/Os are provided, you can easily connect a variety of peripherals using jumper wire or plug the module in HA-MB02 Digital Circuits Lab Platform. The pocket-sized dimension makes it a good choice for you when a FPGA core board is needed in your project. A USB to UART converter is integrated for easy data communication with PC. This guide will briefly describe the hardware modules on this board, so as to help you make better use of it.

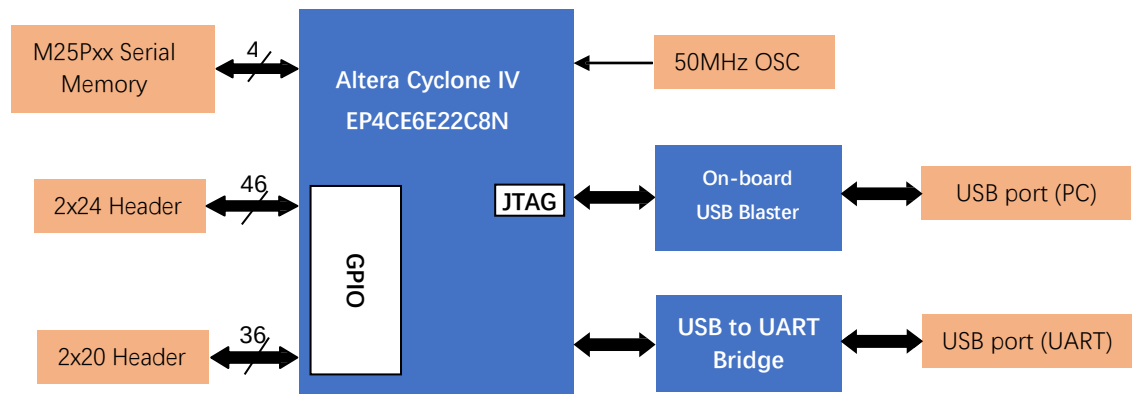
Features:

- Altera Cyclone IV device—EP4CE6E22C8N
- USB to UART
- 88 expansion header (82 I/Os, +3.3V, GND)
- All I/Os with ESD chip protection
- On-board USB Blaster
- External serial configuration device: M25Pxx
- Reset pushbutton
- 50 MHz clock oscillator
- USB power supply
- Very compact board size: 87(mm) x 55(mm)



2. Hardware description

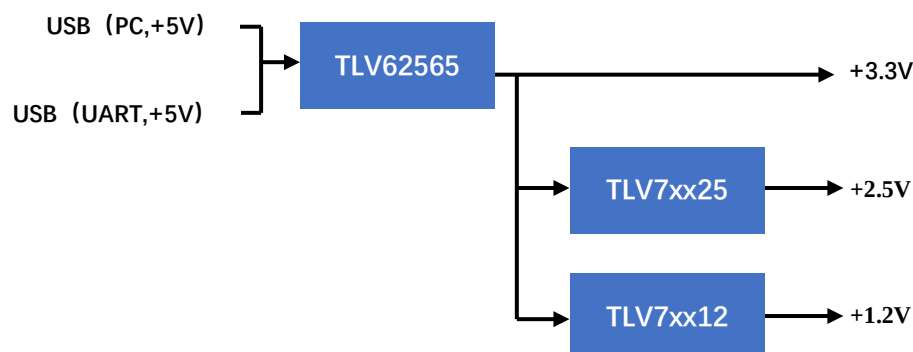
HA-EDA01 FPGA Module contains several parts that are easy to understand. The block diagram shown below depicts the architecture of this board.



HA-EDA01 FPGA Module Block Diagram

2.1. Power supply

HA-EDA01 FPGA Module could be powered with USB(PC) port(+5V DC, at least 500mA) or an external supply through USB(UART) port. Three LDOs are used to regulate down the input power to +3.3V, +1.2V and +2.5V respectively.



Note: Do not connect a power higher than +3.3V to any IOs of this board. This may accidentally damage the input capacitors.

2.2. FPGA Device

HA-EDA01 FPGA Module includes a Cyclone IV FPGA device — EP4CE6E22C8N housed in a 144-Pin TQFP package. This device features higher amount of logic and memory resources compared to older Cyclone devices. You can easily implement hardware multiple logic circuits on this device. NIOS II microcontroller is also supported. The table below has an overview of the resources for this device.

Resources	EP4CE6
Logic elements (LEs)	6,272
Embedded memory (Kbits)	270
Embedded 18 × 18 multipliers	15
General-purpose PLLs	2
Global Clock Networks	10
User I/O Banks	8

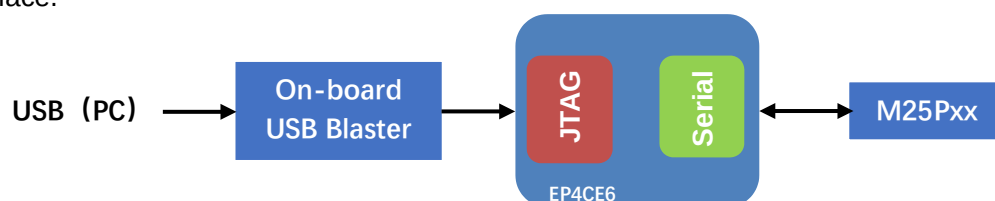
The table below shows the power pins connection for this device on HA-EDA01 FPGA Module.

Power Pins Connection

Power Pin Name	Power Rail	LDO
VCCIO1-VCCIO8	+3.3V	TLV62565
VCCINT	+1.2V	TLV7xx12
VCCA1,VCCA2	+2.5V(Filtered)	TLV7xx25
VCCD_PLL1,VCCD_PLL2	+1.2V(Filtered)	TLV7xx12

2.3. On-board USB Blaster and External Serial Configuration Device

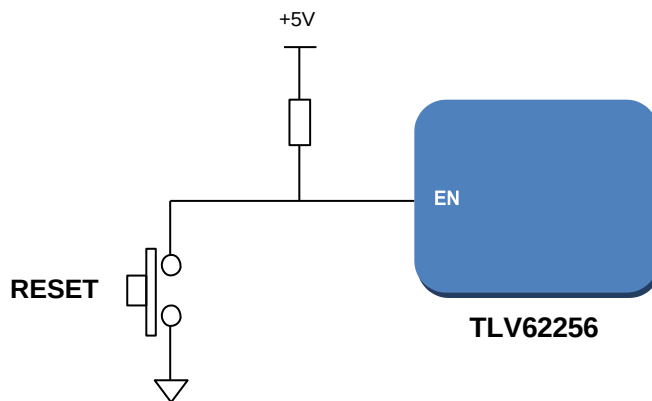
The internal SRAM of FPGA device could be programmed via On-board USB blaster. A nonvolatile serial configuration device M25Pxx is assembled on this board. The configuration file will be programmed to serial device via On-board USB blaster. In this way, the FPGA device acts as a flash loader. The JTAG LED will be blink when the programming process is active. Please refer to the **Quartus II Software Quick Start Guide** for details about how to program the external serial configuration device via JTAG interface.



2.4. Reset Button

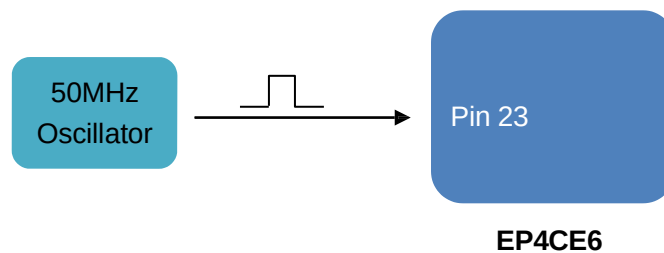
A Reset pushbutton is available on HA-EDA01 FPGA Module. This button is useful when you want to reinitialized the module. It force the FPGA device to reload

configuration file from external serial device.



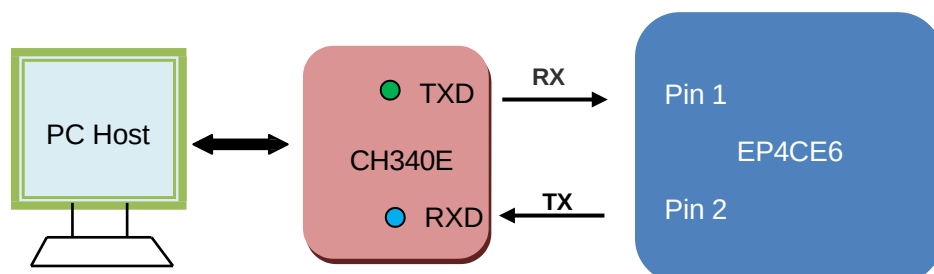
2.5. Clock Oscillator

HA-EDA01 FPGA Module includes one 50MHz clock oscillator. It can be used as a global clock source or drive the internal PLL of FPGA device.



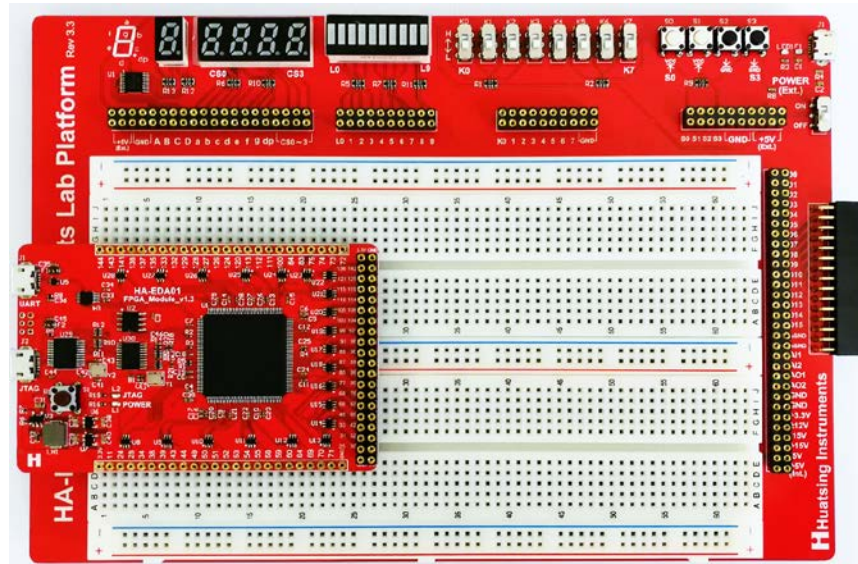
2.6. USB to UART Bridge

Serial communication can be easily implemented and is widely used when data exchange is needed between PC and peripherals. Since most new generation PCs are not assembled with an older 9-Pin D-Sub serial port. But USB port is abundant. The USB to UART converter IC solves the problem while retaining the advantage of serial port. CH340E is used in this board to play a role of USB to UART converter.



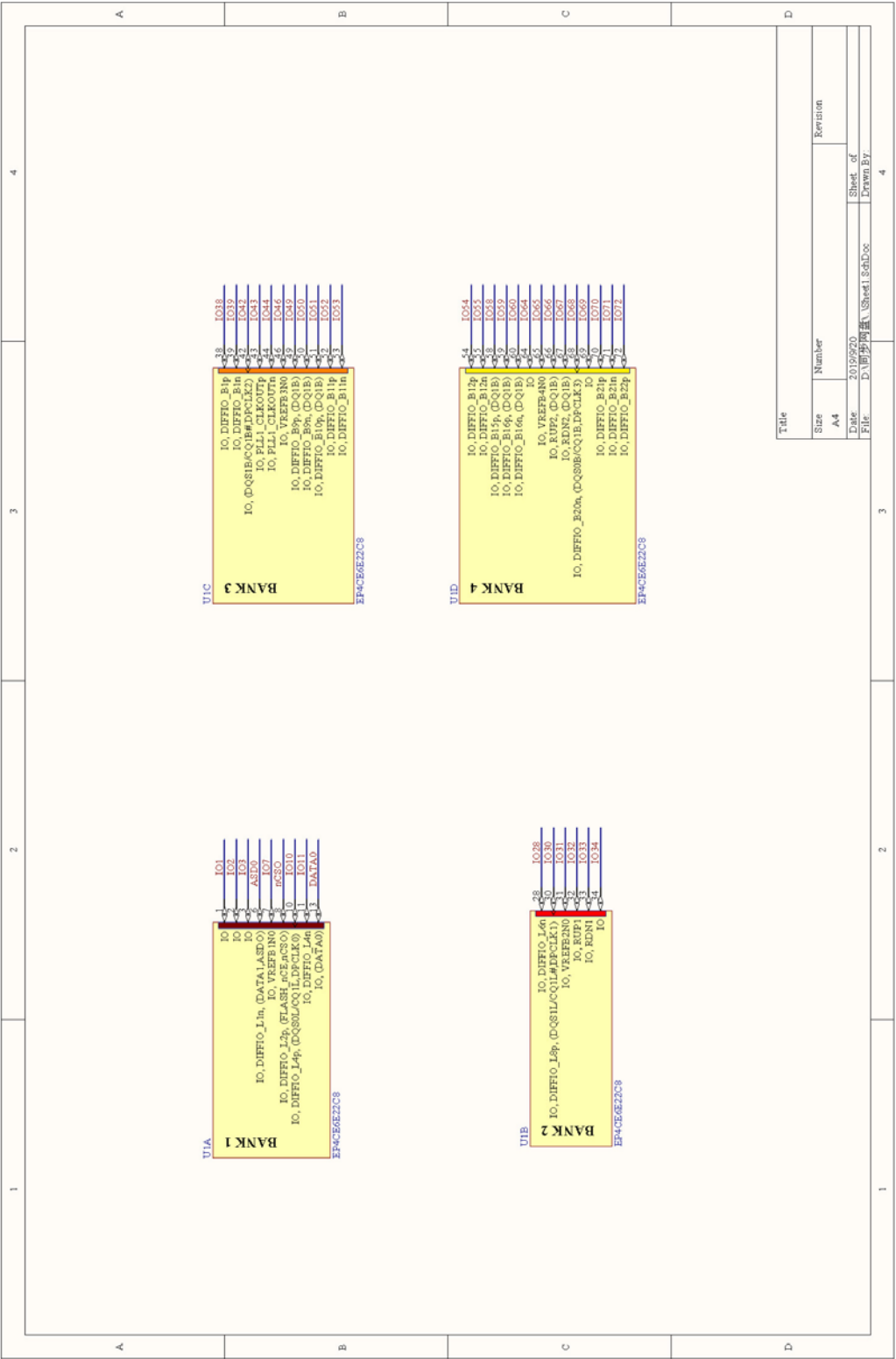
2.7. Expansion Header

Two groups of expansion header are available. 2x24 header includes 46 I/Os and +3.3V power supply, can connect with HA-MB01 or Jumper wire. 2x20 header includes 36 I/Os and +3.3V power supply, can only connect with Jumper wire.



HA-EDA01 FPGA Module plug on HA-MB02 Digital Circuits Lab Platform with 2x24 Header

3. Schematics



1	2	3	4
A	B	C	D
U10 BANK 7 IO, DIFFIO_T2p, (DQST/CLKOUT/CLKO) IO, DIFFIO_T1p IO, PLL2_CLKOUTn IO, PLL2_CLKOUTp IO, RUP4, (DQIT) IO, RDN4, (DQIT) IO, VREFB7N0 IO, DIFFIO_T1n, (DQIT) IO, DIFFIO_T1n IO, DIFFIO_T1n IO, DIFFIO_T1n IO, DIFFIO_T1n IO, DIFFIO_T1n IO, DIFFIO_T1n IO, DIFFIO_T1n U11 BANK 8 IO, DIFFIO_T1a IO, DIFFIO_T1p IO, DIFFIO_T1n, (DQIT) IO, DIFFIO_T1n, (DATA3), (DQIT) IO, DIFFIO_T3a, (DQIT) IO, VREFB8N0 IO, (DATA5), (DQIT) IO, (DATA6) IO, DIFFIO_T3p, (Q08IT/CLKOUT/CLKO) IO, DIFFIO_T1n, (DQIT) IO, DIFFIO_T1p, (DMIT) U1F BANK 5 IO, DIFFIO_R4p, (CRC_ERROR) IO, DIFFIO_R3p, (GCEO) IO, DIFFIO_R3p, (CLUSER) IO, (DQSG0/CLKOUT) U1F BANK 6 IO, DIFFIO_R4p, (UNIT_DONE) IO, DIFFIO_R4p, (CRC_ERROR) IO, DIFFIO_R3p, (GCEO) IO, DIFFIO_R3p, (CLUSER) IO, (DQSG0/CLKOUT) U10 BANK 7 IO, DIFFIO_T2p, (DQST/CLKOUT/CLKO) IO, DIFFIO_T1p IO, PLL2_CLKOUTn IO, PLL2_CLKOUTp IO, RUP4, (DQIT) IO, RDN4, (DQIT) IO, VREFB7N0 IO, DIFFIO_T1n, (DQIT) IO, DIFFIO_T1n IO, DIFFIO_T1n IO, DIFFIO_T1n IO, DIFFIO_T1n IO, DIFFIO_T1n IO, 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